Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2677	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/09 08:20
L2	51	L1 and mcm with "circuit board"	US-PGPUB; USPAT	OR	ON	2005/09/09 08:39
L3	2	mcm with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:40
L4	2677	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/09 08:48
L5	2	L4 and "flip chip" with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:52
L6	32	"flip chip" with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:53
L7	5	"flip-chip" with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:56
L8	32	"flip-chip type" with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:58
L9	7	(flip-chip type) with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 08:59
L10	15	(flip-chip mounting) with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 09:00
L11	32	"flip-chip mounting" with ((active and passive) adj chip)	US-PGPUB; USPAT	OR	ON	2005/09/09 09:00
L13	10	(("6504746") or ("6404062") or ("6809421") or ("6356453") or ("6607938") or ("6864588") or ("6239496") or ("6833628") or ("6376917") or ("6737295")).PN.	USPAT; USOCR	OR	OFF	2005/09/09 11:19
S1	11458	"multichip module" or "MCM"	US-PGPUB; USPAT	OR	ON	2005/09/07 10:31
S2	13201	"multichip module" or "MCM"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:22
S3	1483	S2 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:22
S4	48	S3 and "multilayer interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:25

S5	7	S4 and "bonding pads"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:23
S6	3	S5 and plugs	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:24
S7	6386	((438/106,107,108) or (257/516, 678,734,758)).CCLS.	USPAT; USOCR	OR	OFF	2005/09/01 12:52
S8	427	S7 and ("multichip module" or "mcm")	US-PGPUB; USPAT	OR	ON	2005/09/01 12:26
S9	8933	S7 and "multichip module" or "mcm"	US-PGPUB; USPAT	OR	ON	2005/09/01 12:27
S10	842	S9 and "bonding pads"	US-PGPUB; USPAT	OR	ON	2005/09/01 12:27
S11	122	S10 and plugs	US-PGPUB; USPAT	OR	ON	2005/09/01 12:33
S12	324	(mcm or multichip or multi adj chip) with "module package"	US-PGPUB; USPAT	OR	ON	2005/09/01 12:34
S13	339	(mcm or multichip or multi adj chip) with "module package"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:34
S14	4531256	S13 and (substrate with "insulating layer" with "multilayer interconnection" with plugs with "bonding pads")I	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:37
S15	0	S13 and substrate with "insulating layer" with "multilayer interconnection" with plugs with "bonding pads"I	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:38
S16	349556	S13 and substrate on "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:38
S17	294	S13 and (substrate on "insulating layer")	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:39

S18	294	S13 and ("insulating layer" on substrate)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:39
S19	34	S18 and ("multilayer interconnection" on "insulating layer")	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:05
S20	915	S9 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:45
S21	35	S20 and "multilayer interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:45
S22	460	S20 and "interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:45
S23	128	S22 and "bonding pads"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:46
S24	26	S23 and plugs	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:46
S25	110	S23 and via	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:46
S26	25	S25 and plugs	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:46
S27	13602	((438/106,107,108) or (257/516, 678,734,758,700)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/09/01 12:53
S28	9019	S27 and "multichip module" or "mcm"	US-PGPUB; USPAT	OR	ON	2005/09/01 12:53

S29	10377	S27 and "multichip module" or "mcm"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:01
S30	941	S28 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:55
S31	36	S30 and "multilayer interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 12:55
S32	375	S27 and "multichip module"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:01
S33	1	S32 and "second surface" with "third bonding pads"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:02
S34	354	S32 and chips	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:03
S35	9	S34 and pads with plugs	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:03
S36	0	S34 and "pads with plugs"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:03
S37	9	S34 and (pads with plugs)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:03
S38	32	S34 and (pads and plugs)	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 13:03

S39	13602	((438/106,107,108) or (257/516, 678,734,758,700)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	OFF	2005/09/01 15:31
S40	375	S39 and "multichip module"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 15:31
S41	151305	"insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:06
S42	211	S41 and "multilayer interconnection structure"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:32
S43	17	S42 and "bonding pads"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:06
S44	64	S42 and chip	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:13
S45	55	S42 and plug	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:17
S46	53	S40 and ((passive and active) with (device or chip))	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/01 16:17
S47	951008	semiconductor	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:32
S48	467199	S47 and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:33

S49	2535567	S48 and insulating layer	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:34
S50	66495	S48 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:34
S51	166	S50 and "multilayer interconnection structure"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:35
S52	22	S51 and ("conductive plugs" or "conductive paste" or "conductive material fills via holes")	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:46
S53	4	S52 and "bonding pads"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:36
S54	78	"multichip substrate"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:55
S55	13	S54 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:58
S56	289	"multilayer interconnection" with "integrated circuit"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 13:59
S57	77	S56 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 14:05
S58	16	S57 and plugs	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 14:00

S59	13201	"multichip module" or "MCM"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 14:05
S60	78	S59 and "multilayer interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 14:06
S61	48	S60 and "insulating layer"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/02 15:32
S62	4606	(257/778,777,685,686,737,780).CCLS.	USPAT; USOCR	OR	OFF	2005/09/02 15:33
S63	2668	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/02 15:35
S64	18323	flip adj chip	US-PGPUB; USPAT	OR	ON	2005/09/02 15:35
S65	1347	S63 and flip adj chip	US-PGPUB; USPAT	OR	ON	2005/09/02 15:36
S66	1347	S63 and "flip chip"	US-PGPUB; USPAT	OR	ON	2005/09/09 08:48
S67	156	S66 and interposer	US-PGPUB; USPAT	OR	ON	2005/09/02 15:50
S68	2677	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/06 09:42
S69	0	S68 and MCM with "package substrate" with "integrated circuit chip"	US-PGPUB; USPAT	OR	ON	2005/09/06 09:42
S70	6	S68 and (MCM with "integrated circuit chip")	US-PGPUB; USPAT	OR	ON	2005/09/06 09:45
S71	2279	S68 and ("integrated circuit chip" with package substrate)	US-PGPUB; USPAT	OR	ON	2005/09/06 09:46
S72	12	S68 and ("integrated circuit chip" with "package substrate")	US-PGPUB; USPAT	OR	ON	2005/09/06 13:41
S73	7	(("4394712") or ("4807021") or ("4897708") or ("4954875") or ("5202754") or ("5229647") or ("5767001")).PN.	USPAT; USOCR	OR	OFF	2005/09/06 14:16
S74	7	(("5065505") or ("5396403") or ("5477082") or ("5977640") or ("6075287") or ("6133637") or ("6150724")).PN.	USPAT; USOCR	OR	OFF	2005/09/06 14:17

S75	289	"multilayer interconnection" with "integrated circuit"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:31
S76	3317	"multilayer interconnection"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:31
S77	6	S76 and "one integrated circuit device"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:33
S78	4	S76 and "includes integrated circuit"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:35
S79	0	"multilayer interconnection structure includes integrated circuit"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:36
S80	0	"integrated circuit in a multilayer interconnection structure"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:36
S81	0	"integrated circuit device in a multilayer interconnection structure"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:39
S82	51911	"integrated circuit device"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:39
S83	92	S82 and "multilayer interconnection structure"	US-PGPUB; USPAT; USOCR; EPO; JPO; IBM_TDB	OR	ON	2005/09/06 15:40
S84	2677	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/07 10:31
S85	1352	S84 and "flip chip"	US-PGPUB; USPAT	OR	ON	2005/09/07 10:31
S86	156	S85 and interposer	US-PGPUB; USPAT	OR	ON	2005/09/07 10:31

S87	1	S86 and "multilayer interconnection"	US-PGPUB; USPAT	OR	ON	2005/09/07 10:34
S88	5	S85 and "multilayer interconnection"	US-PGPUB; USPAT	OR	ON	2005/09/07 13:33
S89	4	S88 and insulating	US-PGPUB; USPAT	OR	ON	2005/09/07 13:33
S90	2677	(257/778,777).CCLS.	USPAT; USOCR	OR	OFF	2005/09/08 08:56
S91	1352	S90 and "flip chip"	US-PGPUB; USPAT	OR	ON	2005/09/08 08:56
S92	156	S91 and interposer	US-PGPUB; USPAT	OR	ON	2005/09/08 08:56
S93	0	S92 and substrate adj3 thickness adj3 "10 to 500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 08:56
S94	152	S92 and substrate thickness adj3 "10 to 500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:00
S95	0	"thickness of semiconductor substrate" with "10 to 500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:02
S96	0	"thickness of semiconductor substrate"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:02
S97	18632	"thickness substrate"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:02
S98	2	"10 micron meter" with "500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:04
S99	0	S97 and "10 micron meter" with "500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:03
S100	0	"10 to 500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05
S101	1	"substrate thickness" with """500"" micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05
S102	1	"substrate thickness" with "500 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05
S103	0	"substrate thickness" with "10 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05
S104	0	"substrate thickness" with "1150 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05
S105	0	"substrate thickness" with "150 micron meter"	US-PGPUB; USPAT	OR	ON	2005/09/08 09:05